Optimising Quantum Comparator Circuits by Minimising T-gate Count

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ABSTRACT
Quantum comparators play a significant role within the scientific community, serving as essential components in a variety of algorithms. Our study introduces a novel approach by delving into the realm of comparator circuits, with a specific focus on three distinct designs found in existing literature. These circuits stand out for their utilisation of T-gates, which have garnered attention in circuit design due to their capacity to facilitate the implementation of error-correcting codes. However, it is crucial to acknowledge that T-gates entail a substantial computational overhead. One of the primary contributions of our research lies in optimising the quantum gates utilised within these circuits. We propose circuits employing Clifford+T gates - a universal set comprising Pauli gates, H, T, CNOT, and S gate - to enable error correction code implementation while minimising the usage of T-gates, thereby reducing computational expenses and enhancing circuit resilience against errors and external disturbances. This optimisation is important for mitigating the impact of internal and external noise.

CCS CONCEPTS
• Computer systems organization → Quantum computing.

KEYWORDS
Quantum Computing, T-gates, Clifford+T, Quantum Comparators

1 INTRODUCTION
In recent years, quantum computing has emerged as a promising solution to overcome classical computer limitations in the Post-Moore era. In the current era of Noisy Intermediate-Scale Quantum (NISQ) computing, we encounter challenges such as limited resources and difficulties in implementing fault-tolerant circuits [9]. Despite having a moderate number of qubits, quantum computers are not yet efficient in solving significant problems without being affected by noise. Noise presents a significant obstacle, but it can be mitigated through careful circuit design and the incorporation of error correction codes.

The possibilities offered by quantum computing are vast, with an infinite collection of quantum gates available for individual qubit manipulation. This consequently opens up an infinite spectrum of possibilities for cases involving two or more qubits [1]. Particular gate collections such as the Clifford+T set facilitate the approximation of this diversity [2]. Nonetheless, the absence of universality in the Clifford group necessitates the inclusion of the T-gate to constitute the Clifford+T set. While indispensable for noise reduction, incorporating the T-gate leads to increased computational costs and affects circuit efficiency [6, 8]. Our study addresses this by proposing innovative quantum comparator circuits using only Clifford+T gates, chosen for universality and their ability to integrate error correction codes [3, 10]. The accessibility of the Clifford+T set on actual quantum computing platforms further enhances its appeal. We also emphasise efforts to optimise T-gate usage to minimise its impact on circuit design.

2 METHODOLOGY AND OPTIMISATION
The methodology involves a thorough analysis of three quantum comparator circuits documented in the literature, starting with an examination of their gates and progressing towards understanding the circuit’s complete functionality. The primary optimisation revolves around replacing mixed sets of three V-controlled gates with a single Temporary logical-AND gate [5]. This substitution is driven by the fact that a mixed set of three Controlled-V gates performs the same operation as the Temporary logical-AND gate, which is multiplication, but the latter incurs fewer costs in terms of T-gates—both in the required number of T-gates (T-count) and the layers of T-gates needed (T-depth). Specifically, each Controlled-V gate entails a T-count of three and a T-depth of two, whereas the Temporary logical-AND gate requires a T-count of four and a
T-depth of two. Consequently, there is a significant reduction in computational costs related to T-gates.

One of the gates optimised is the Peres gate, whose original version consists of two Controlled-V† gates, one Controlled-V gate, and one CNOT gate. The original implementation can be observed in Figure 1.

The optimised version can be seen in Figure 2. It can be noted that the three Controlled-V gates have been replaced by a Temporary logical-AND gate, and additionally, one CNOT gate has been added.

3 RESULTS

As depicted in Table 1, the proposed circuits show significant improvements in both T-count and T-depth metrics when compared to their original counterparts. This noticeable reduction in T-count and T-depth metrics suggests a considerable enhancement in the efficiency and computational performance of these circuits.

Whilst the optimised circuits do require a slightly increased number of ancillary qubits, the balance between the utilisation of auxiliary qubits and the improved computational efficiency is clearly apparent. These enhancements are achieved exclusively through the utilisation of Clifford+T gates, emphasising a commitment to efficiency and precision in quantum computations. This underscores the potential practical applications of our proposed optimisations in advancing quantum circuit design.

4 CONCLUSIONS AND FUTURE WORK

This study explores three distinct designs of quantum comparator circuits, with a focus on their reliance on T-gates, which are currently gaining attention in quantum circuit design despite their computational costs. Our contribution involves optimizing these circuits by proposing three new quantum comparators utilizing T-gates. This allows for the efficient adaptation of circuits to real quantum platforms, leveraging the advantages of the Clifford+T set while considering their potential for fault-tolerant configurations through error-correcting codes. Additionally, we address the computational overhead associated with T-gates. In future work, scaling up the proposed circuits could enhance practical implementations in quantum computing, facilitating more complex calculations.

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Table 1: Comparison of the studied circuits and proposed circuits in terms of T-count, T-depth and number of ancillary qubits.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>T-count</th>
<th>T-depth</th>
<th>Ancillary</th>
</tr>
</thead>
<tbody>
<tr>
<td>H. Thapliyal et al. [11]</td>
<td>54</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>Optimised proposed circuit 1</td>
<td>24</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>H. Maity [7]</td>
<td>36</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>Optimised proposed circuit 2</td>
<td>16</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>G. Kalita et al. [4]</td>
<td>9</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>Optimised proposed circuit 3</td>
<td>4</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
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REFERENCES